正基科技股份有限公司

AMPAK Technology Inc.

AP5875SA

Evaluation Board User Manual

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Revision

Revision	Date	Description	Revised By
0.1	2024/09/27	Initial released	Gary

Contents

1. EVB Introduction

AP5875SA Evaluation board (EVB) likes as figure1. That is designed for IEEE802.11 a/b/g/n/ac/ax WLAN with integrated Bluetooth application. It is subject to provide a convenient environment for customer's verification on WiFi or Bluetooth function. There are many controller pins and reserved GPIO on Evaluation board which describes as below.

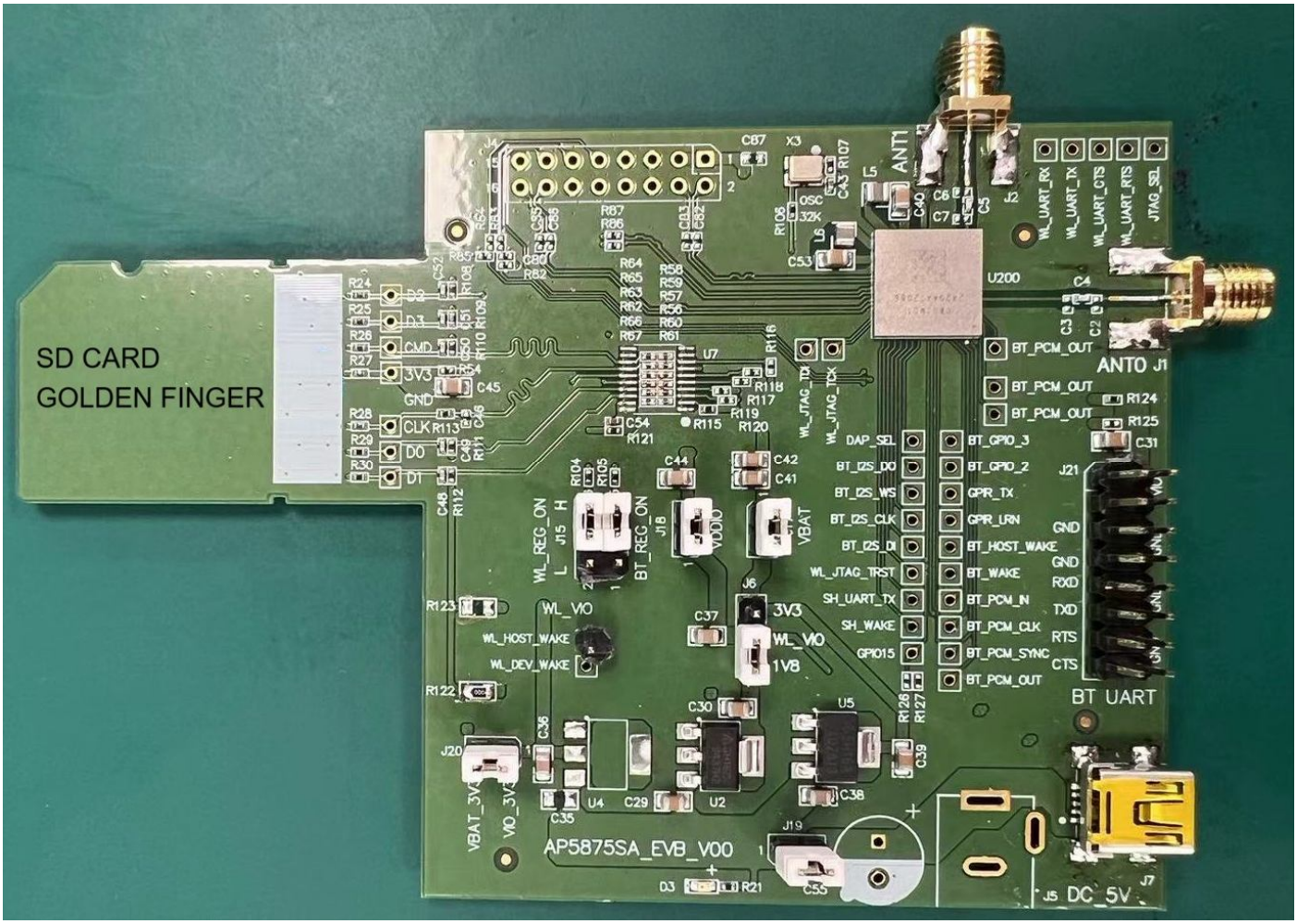

Figure1. Top view of AP5875SA EVB

Interface highlights:

1. U200: AP5875AS SIP module.
2. J21: UART interface connects with UART transport board for BT measuring
3. J15: Enable(H) or disable(L) Bluetooth, WiFi function
4. J17: VBAT power source.
5. J18: VDDIO power source.
6. J7: 5V DC Power input by mini USB.
7. SD card golden finger standard SDIO interfaces for Wi-Fi performance measured.
8. ANT1: SMA connector let RF ANT1 signal in/out path (WiFi and Bluetooth share antenna for AP5875SA), you could connect with RF cable or Dipole antenna.

9. ANT2: SMA connector let RF ANT2 signal in/out path, you could connect with RF cable or Dipole antenna.

2. WiFi Function Verification Step

2.1 WiFi SDIO

Using external pull up resistors depends on the SDIO supply voltage. The resistance range is 30 KΩ~40 KΩ on the four data lines and the CMD line as the following circuitry.

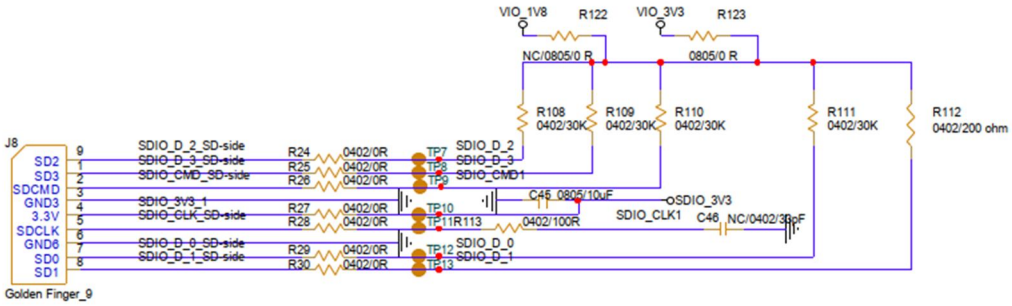

Figure2. WiFi verification connection interface to Host SDIO as using SDIO2.0

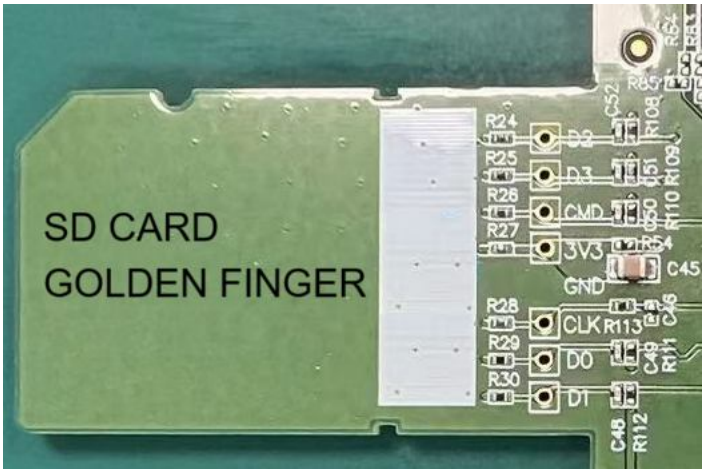

Figure3. EVB interface to HOST SDIO 2.0.

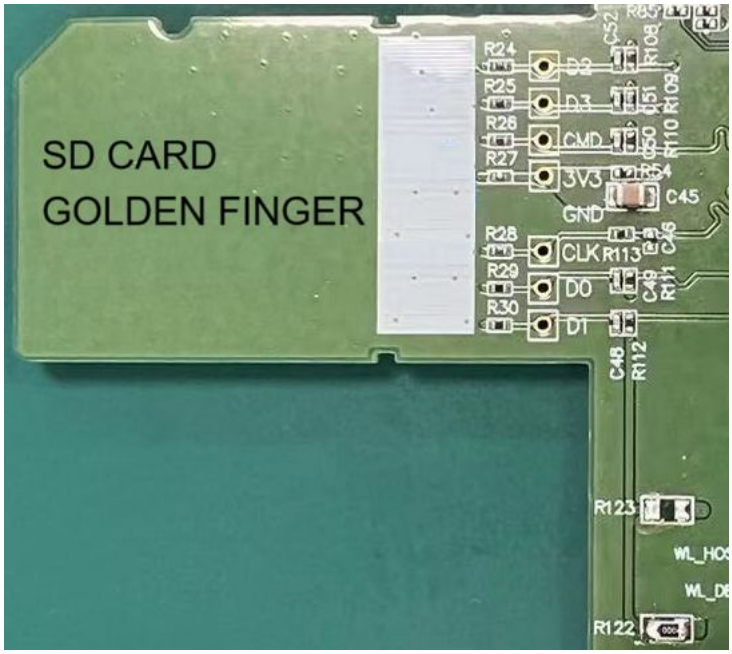

Figure4. EVB interface to HOST SDIO 3.0.

SDIO 2.0 Hardware Setup:

- ✧ Pull up voltage should be 3.3V, so make sure R123 is existed.

SDIO 3.0 Hardware Setup:

- ✧ Pull up voltage should be 1.8V, so make sure R122 is existed.
- ✧ C26/63/64/65/66/67, remove it.

2.2 SDIO Hardware Setup

- ❖ Refer to Figure2 SDIO pin definition connects the J8 interface of AP5875SA evaluation board to Host SDIO control interface.
- ❖ Using pull high resistors (R108, R109, R110, R111, R112) that resistance is 30Kohm for 1.8V or 3.3V VDDIO pull up voltage. (Pull high resistors are un-necessary if at verification phase.)
- ❖ Connects an external antenna at SMA connector on the evaluation board.
- ❖ Note to the VDDIO voltage level should be the same with GPIO voltage level of Host CPU.

2.3 WiFi Software Setup

- ❖ Please follow up software guideline of Ampak official released.

3. Bluetooth Function Verification Step

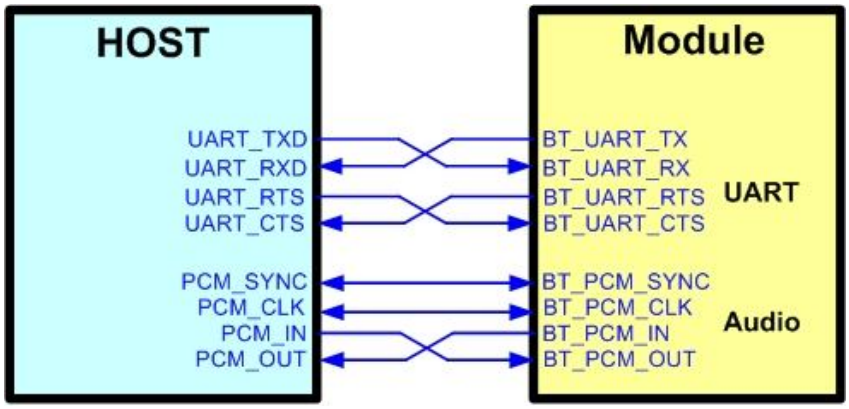

Figure5. Bluetooth verification connection interface to Host UART

Hardware Setup:

- ❖ Refer to Figure5 UART pin definition connects the J21 interface of AP5875SA evaluation board to Host UART control interface.
- ❖ Connects an external antenna at SMA connector on the evaluation board.
- ❖ Note to the VDDIO voltage level should be the same as GPIO voltage level of Host CPU.

WiFi and Bluetooth software setup:

- ❖ Please follow up software guideline of Ampak official released.